Fig. 1A

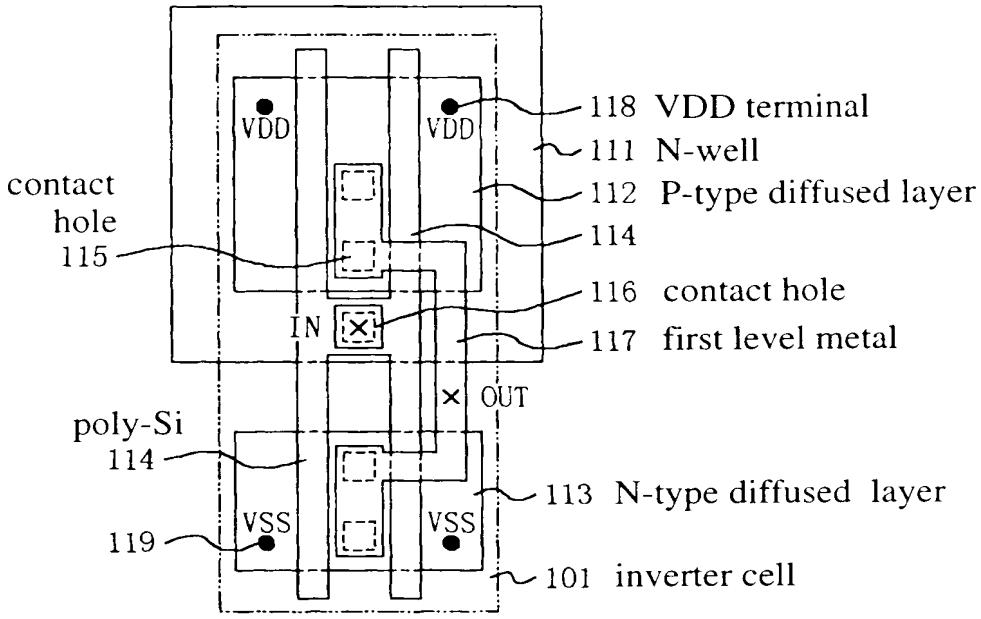
VDD
VDD
118 VDD terminal
111 N-well
contact hole 115
112 P-type diffused layer
114
116 contact hole
IN
117 first level metal
OUT
poly-Si 114
113 N-type diffused layer
VSS
VSS
119
101 inverter cell

Fig. 1B

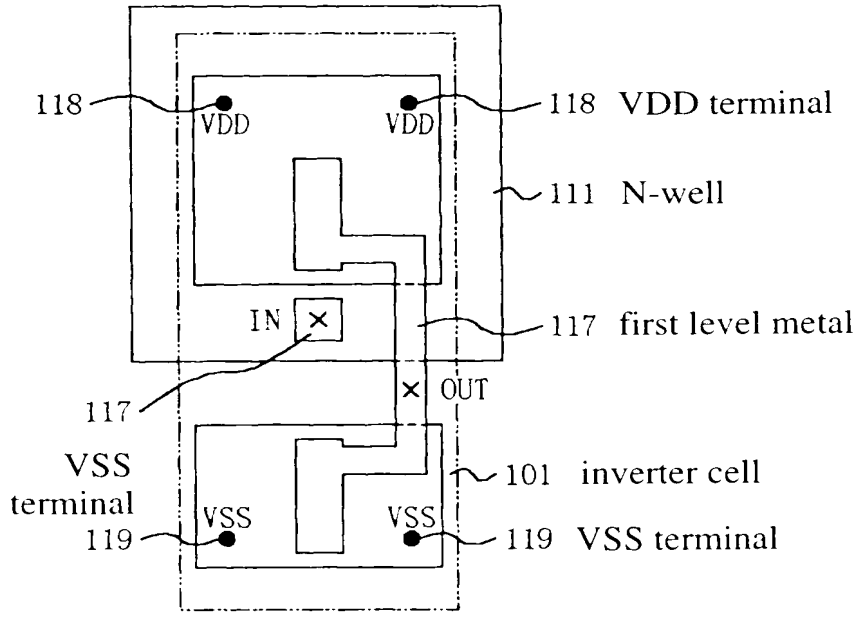
118
VDD
VDD
118 VDD terminal
111 N-well
IN
117 first level metal
OUT
117
VSS terminal 119
VSS
VSS
101 inverter cell
119 VSS terminal

Fig. 2A

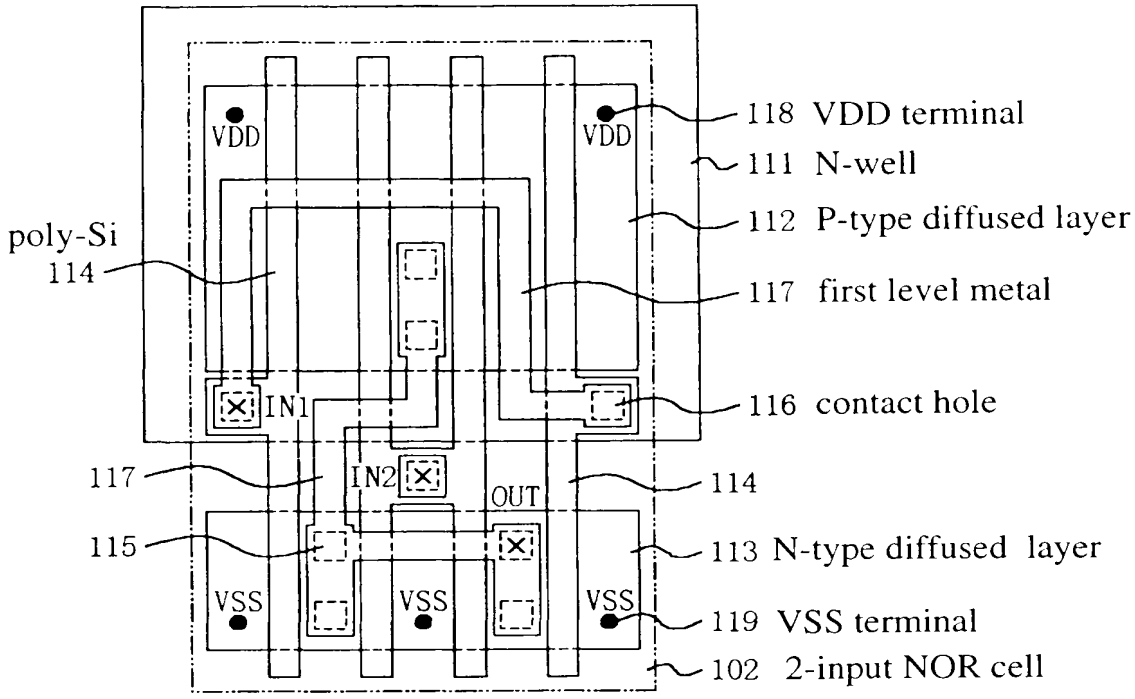
VDD
VDD
118 VDD terminal
111 N-well
112 P-type diffused layer
poly-Si
114
117 first level metal
IN1
116 contact hole
117
IN2
OUT
114
115
113 N-type diffused layer
VSS
VSS
VSS
119 VSS terminal
102 2-input NOR cell

Fig. 2B

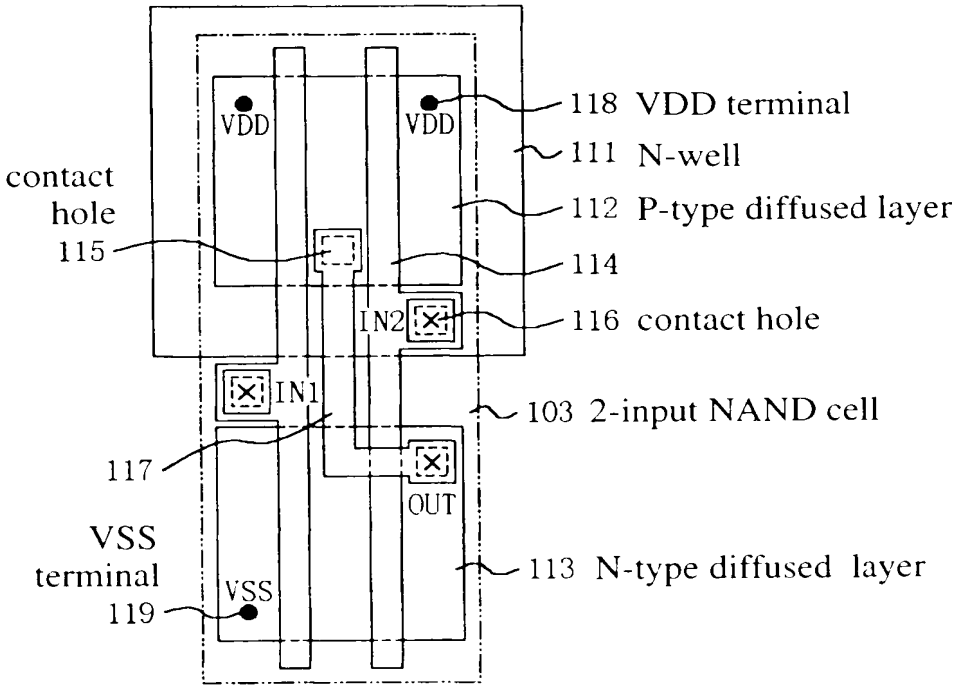
VDD
VDD
118 VDD terminal
111 N-well
contact
hole
115
112 P-type diffused layer
114
IN2
116 contact hole
IN1
103 2-input NAND cell
117
OUT
VSS
terminal
119
VSS
113 N-type diffused layer

Fig. 3A

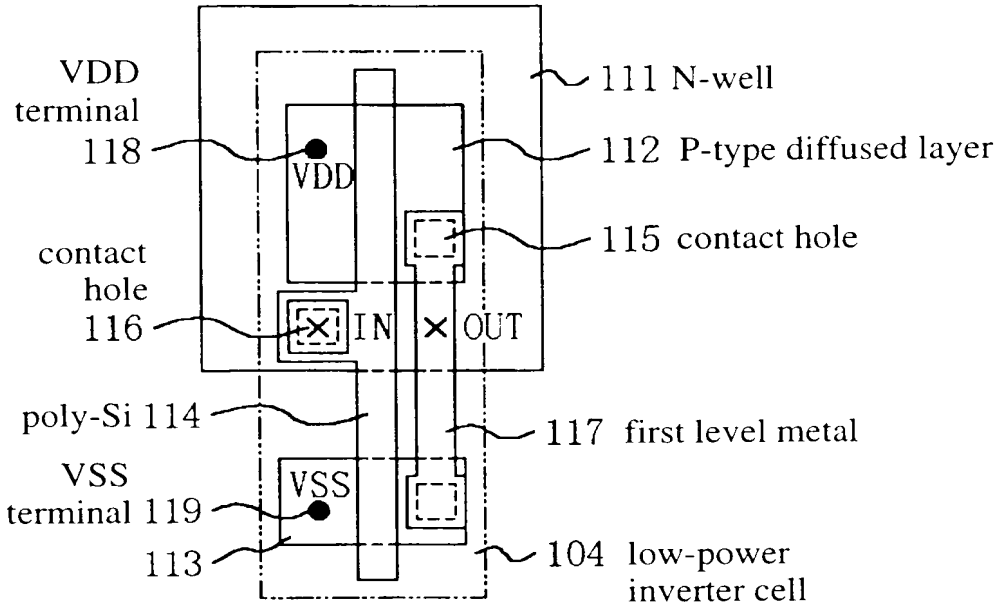
VDD
terminal
118
VDD
111 N-well
112 P-type diffused layer
115 contact hole
contact
hole
116
IN
OUT
poly-Si 114
117 first level metal
VSS
terminal 119
VSS
113
104 low-power
inverter cell

Fig. 3B

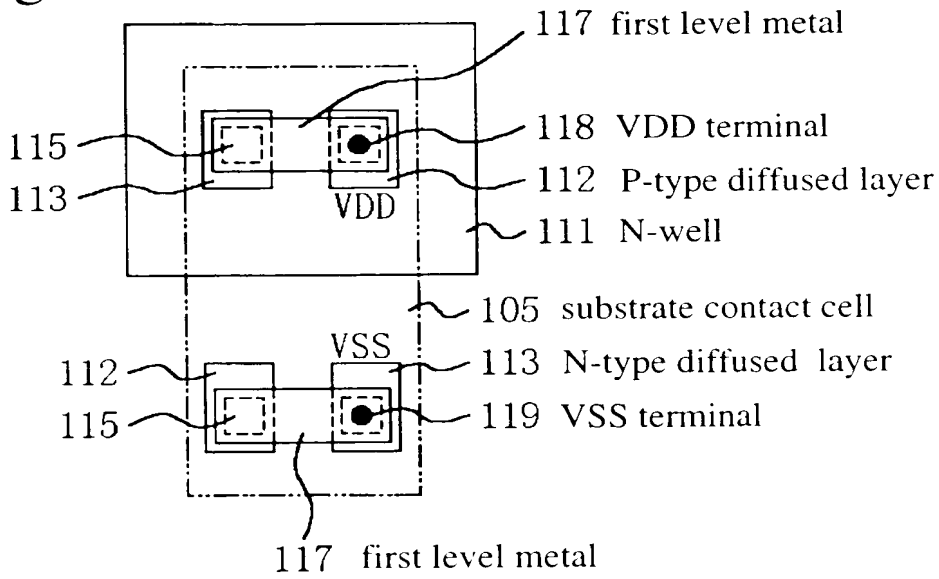
117 first level metal
115
113
118 VDD terminal
112 P-type diffused layer
VDD
111 N-well
105 substrate contact cell
VSS
112
113 N-type diffused layer
115
119 VSS terminal
117 first level metal

Fig. 4

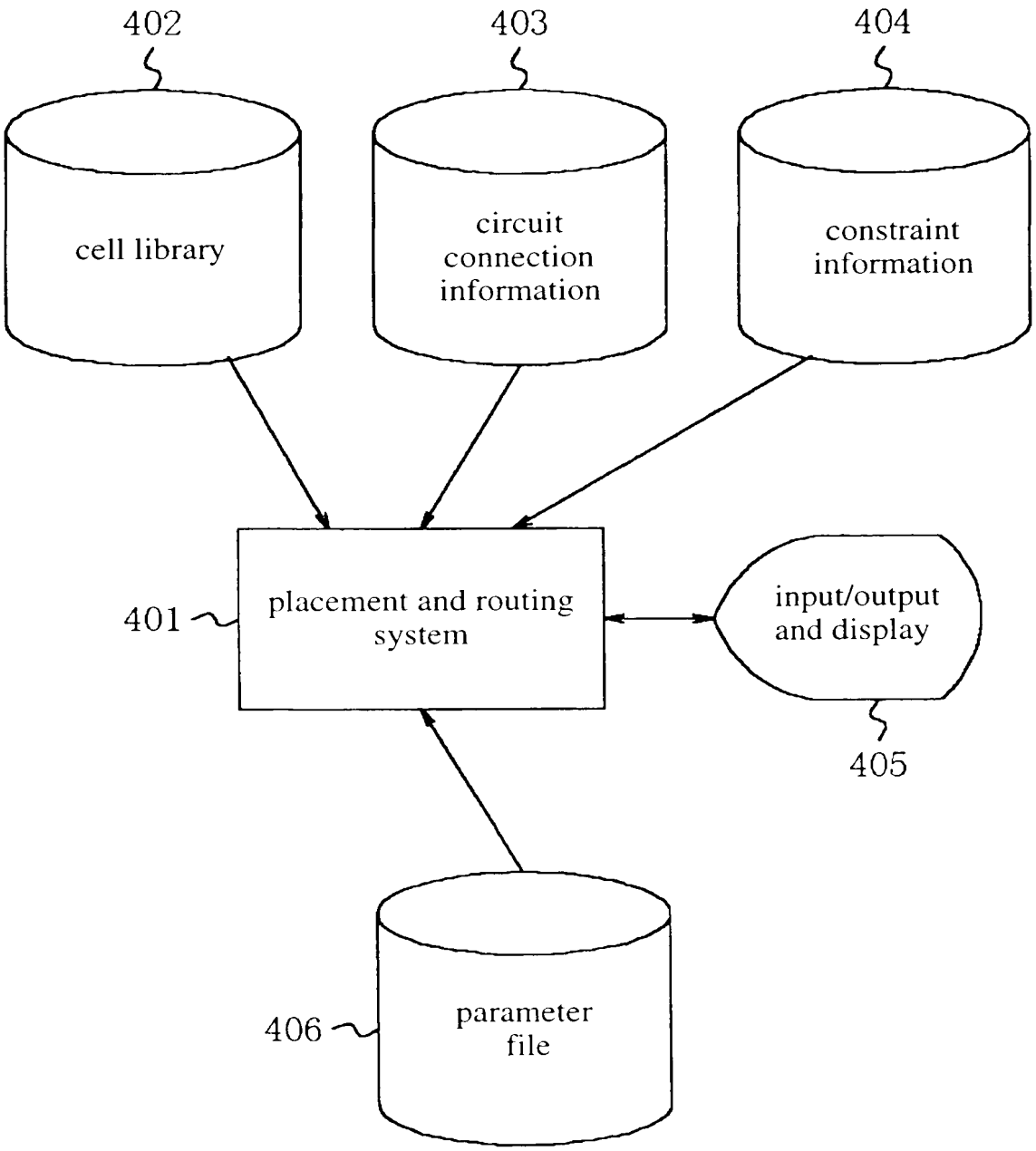
402
403
404
cell library
circuit connection information
constraint information
401
placement and routing system
input/output and display
405
406
parameter file

Fig. 5

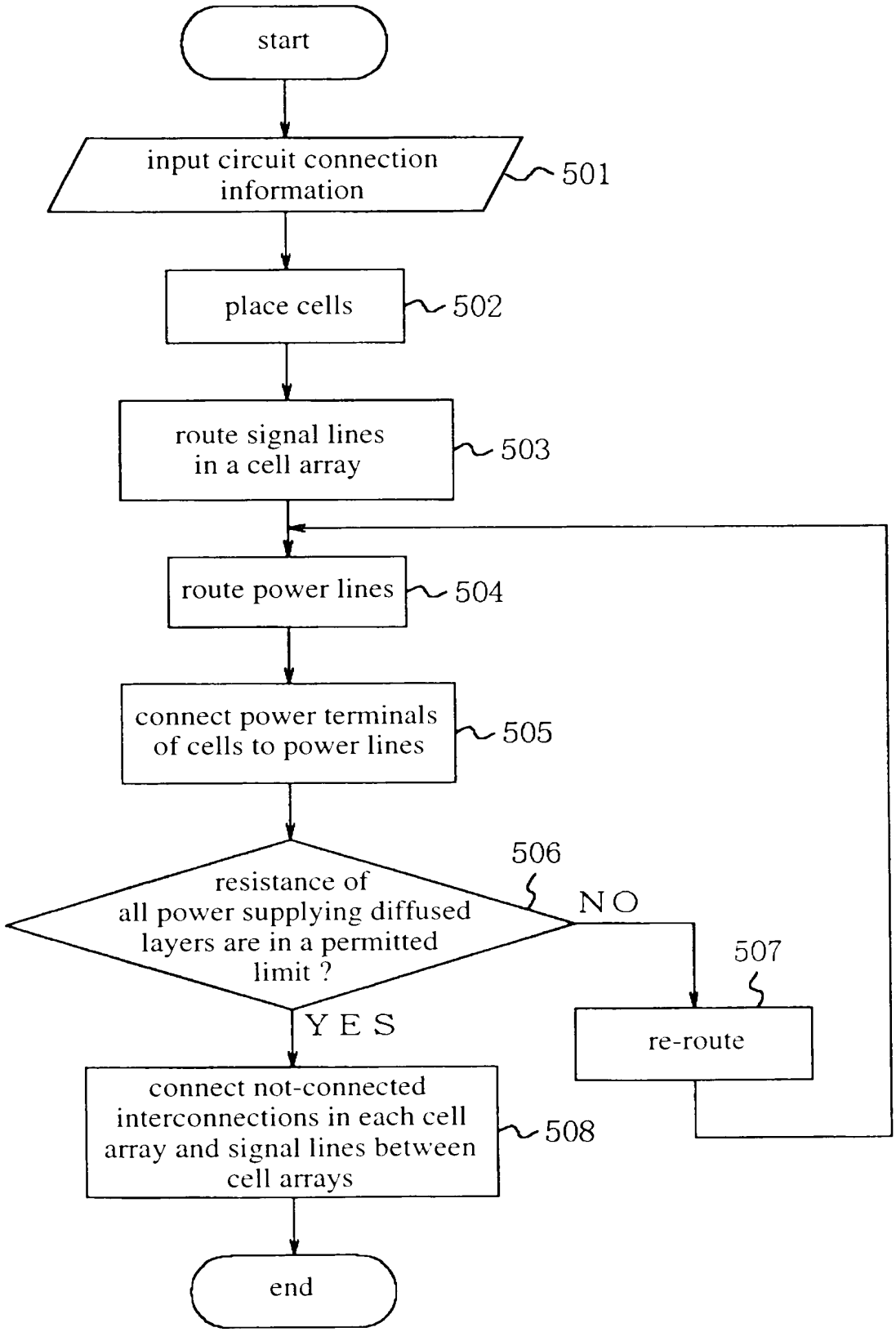
start
input circuit connection information
501
place cells
502
route signal lines in a cell array
503
route power lines
504
connect power terminals of cells to power lines
505
resistance of all power supplying diffused layers are in a permitted limit ?
506
NO
YES
re-route
507
connect not-connected interconnections in each cell array and signal lines between cell arrays
508
end

Fig. 6

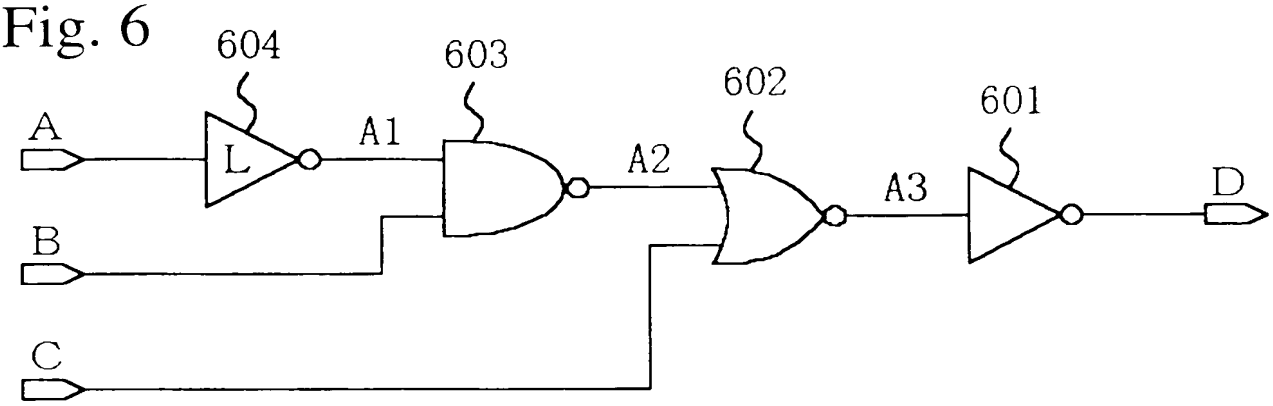
604
603
602
601
A
L
A1
A2
A3
D
B
C

Fig. 12

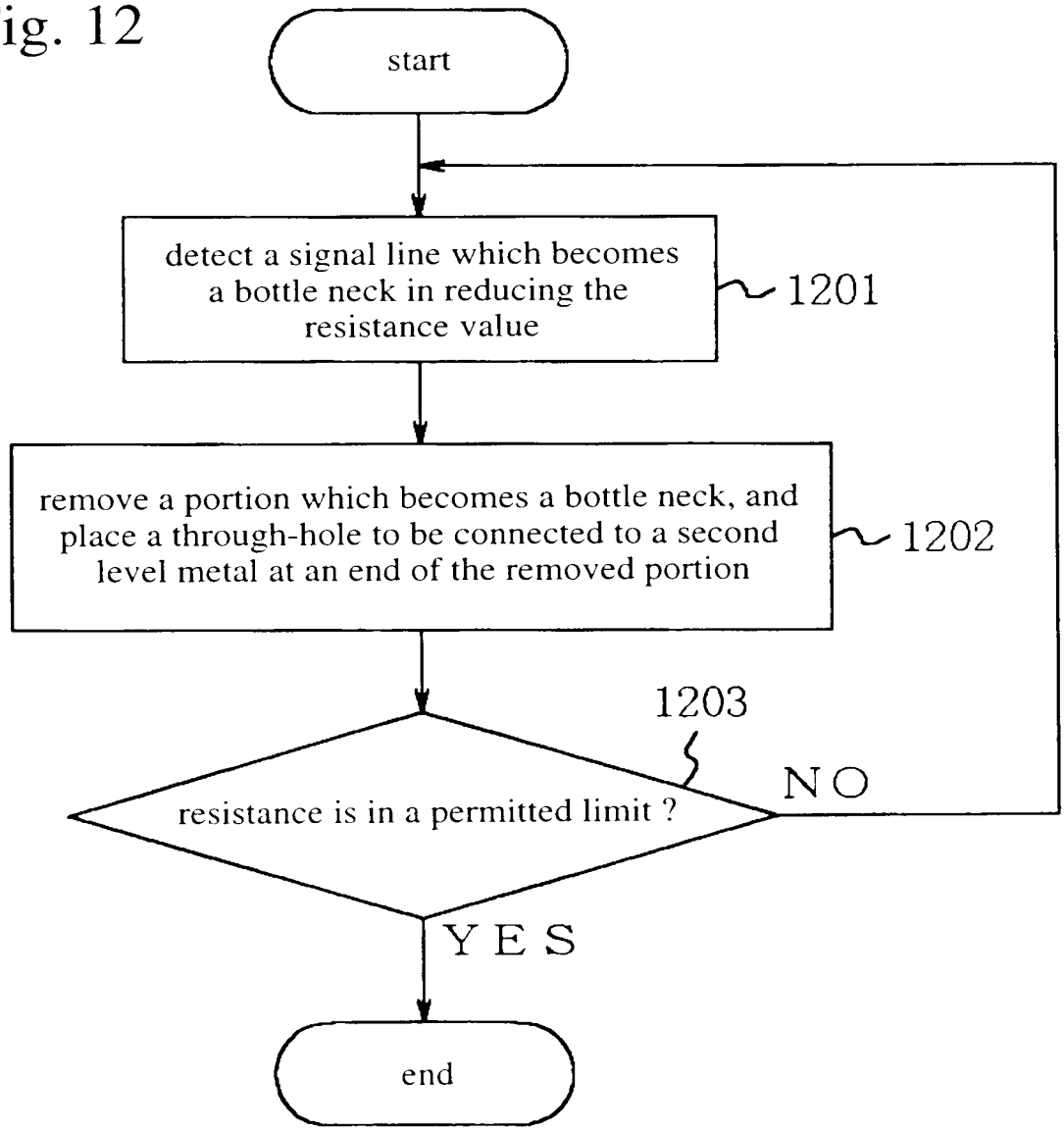
start
detect a signal line which becomes a bottle neck in reducing the resistance value
1201
remove a portion which becomes a bottle neck, and place a through-hole to be connected to a second level metal at an end of the removed portion
1202
1203
resistance is in a permitted limit ?
NO
YES
end

Fig. 7

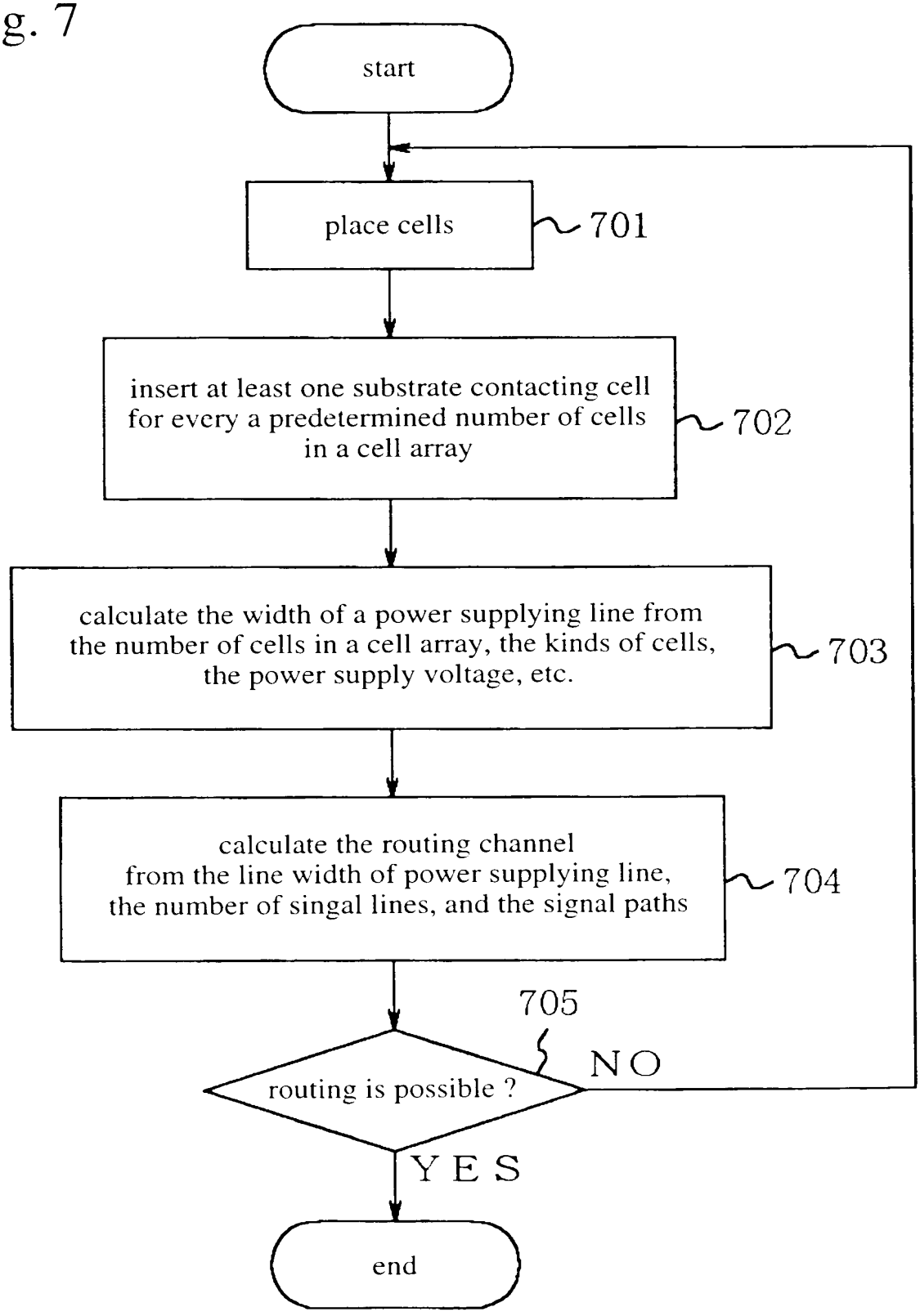
start
place cells
701
insert at least one substrate contacting cell for every a predetermined number of cells in a cell array
702
calculate the width of a power supplying line from the number of cells in a cell array, the kinds of cells, the power supply voltage, etc.
703
calculate the routing channel from the line width of power supplying line, the number of singal lines, and the signal paths
704
705
routing is possible ?
NO
YES
end

Fig. 8

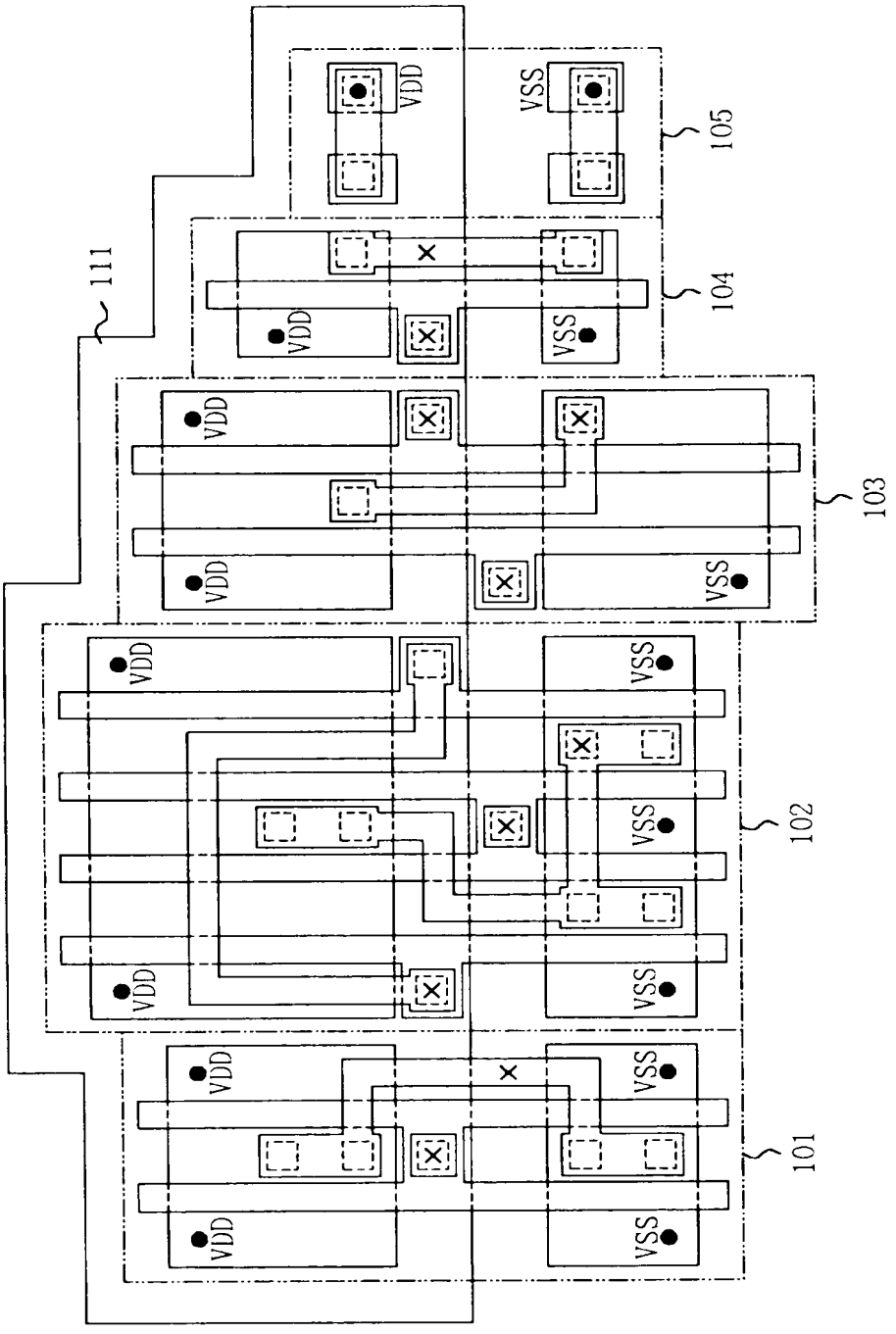

Fig. 9

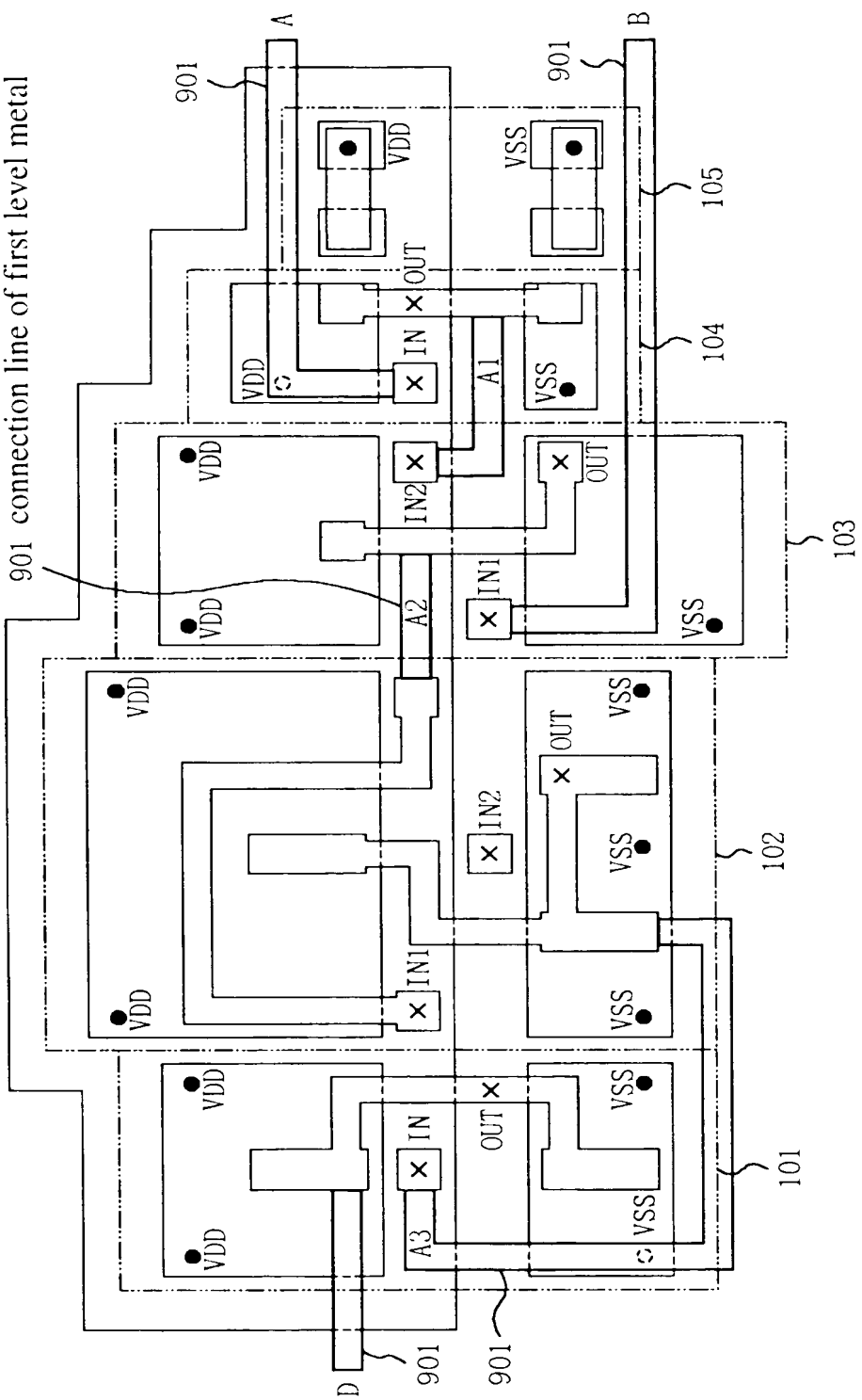
901 connection line of first level metal
A
B
D
901
VDD
VSS
IN
OUT
IN1
IN2
A1
A2
A3
101
102
103
104
105

Fig. 10

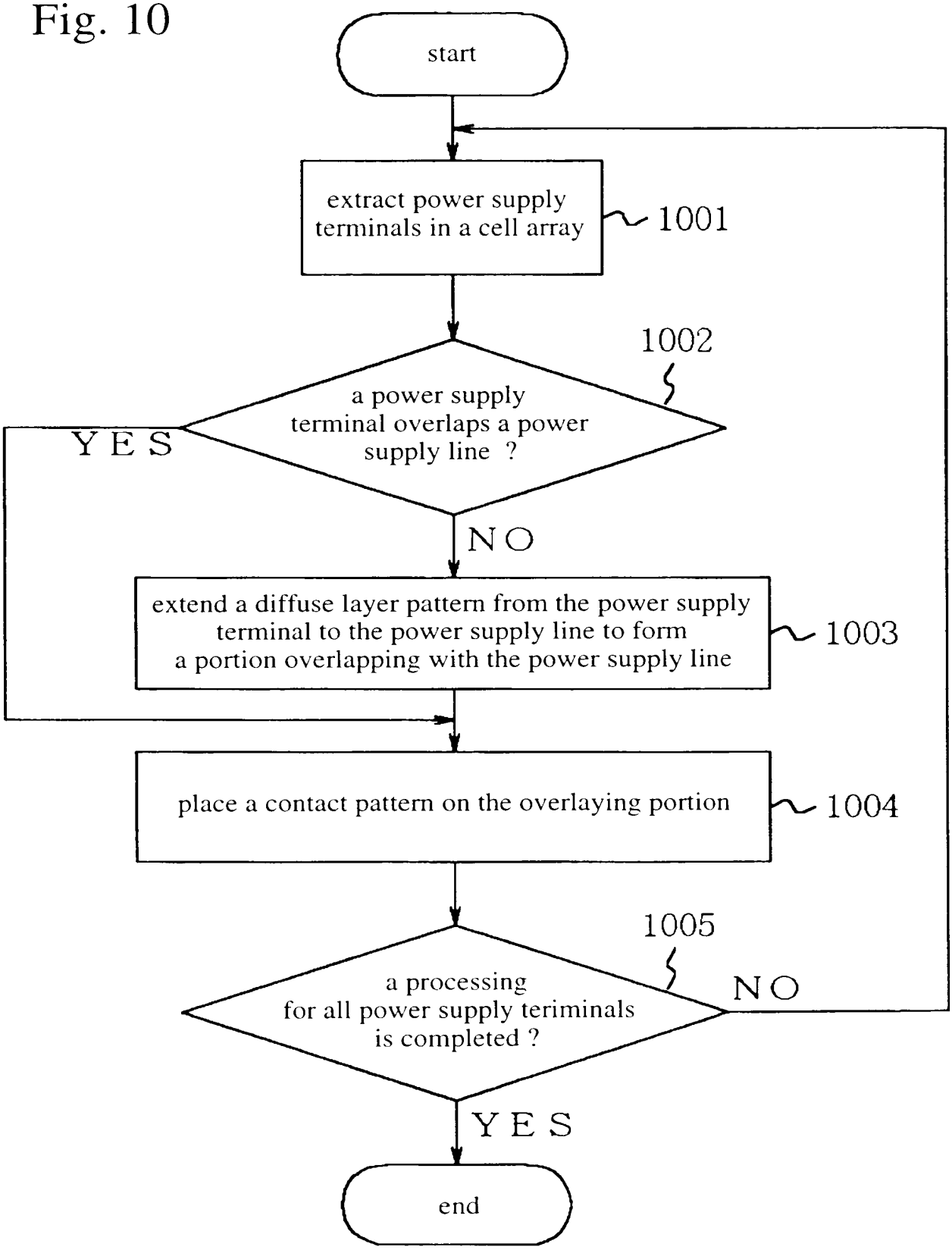
start
extract power supply terminals in a cell array
1001
1002
a power supply terminal overlaps a power supply line ?
YES
NO
extend a diffuse layer pattern from the power supply terminal to the power supply line to form a portion overlapping with the power supply line
1003
place a contact pattern on the overlaying portion
1004
1005
a processing for all power supply teriminals is completed ?
NO
YES
end

Fig. 11

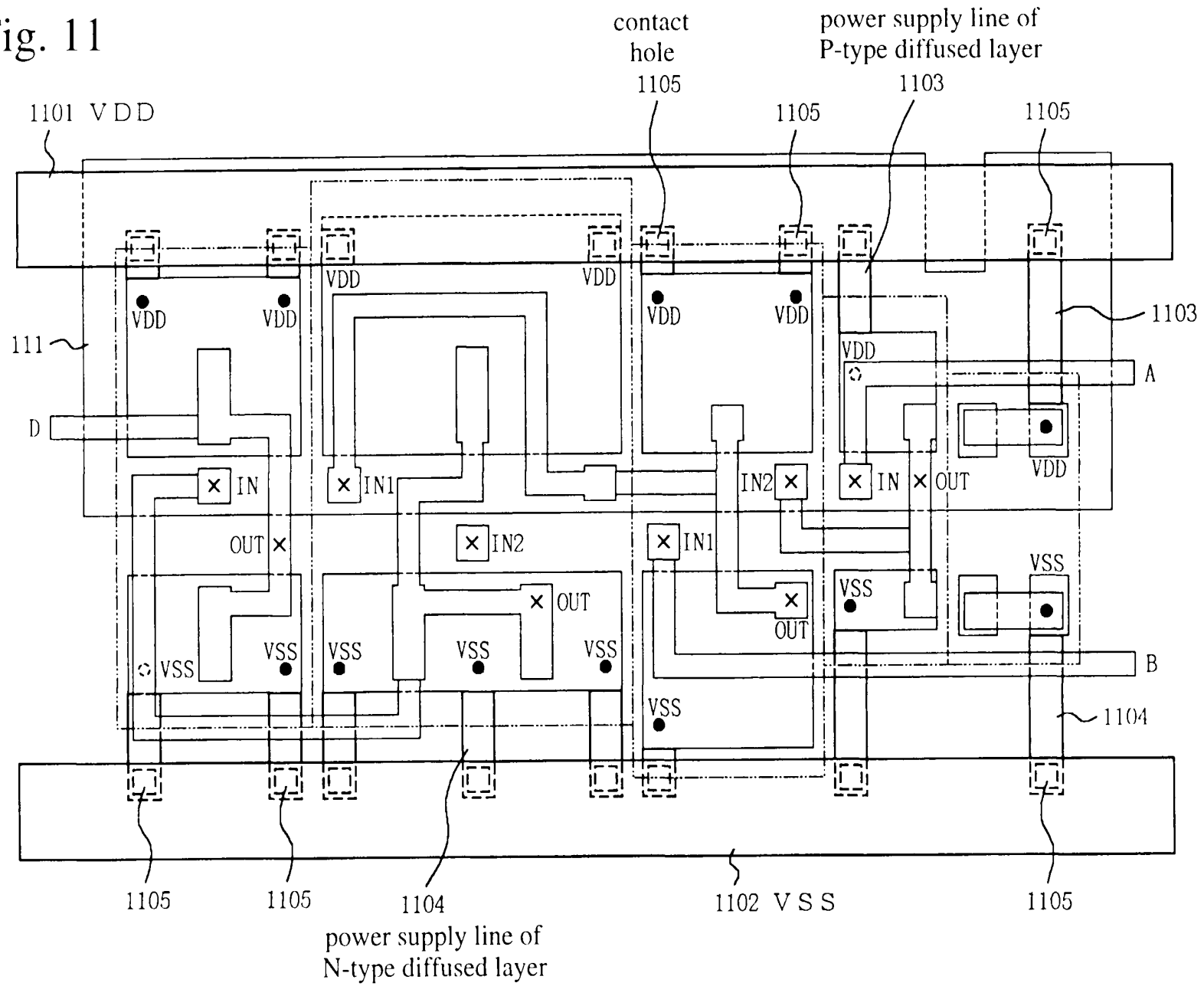
contact hole
1105
power supply line of P-type diffused layer
1103
1101 VDD
1105
1105
1103
VDD
VDD
VDD
VDD
VDD
VDD
VDD
111
A
D
IN
IN1
IN2
IN
OUT
VDD
OUT
IN2
IN1
VSS
OUT
OUT
VSS
VSS
VSS
VSS
VSS
VSS
VSS
B
1104
1105
1105
1104
1102 VSS
1105
power supply line of N-type diffused layer

Fig. 13A

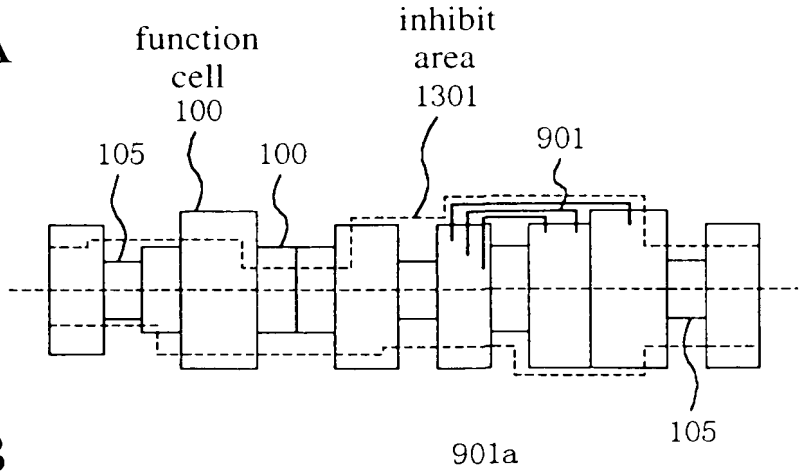

Fig. 13B

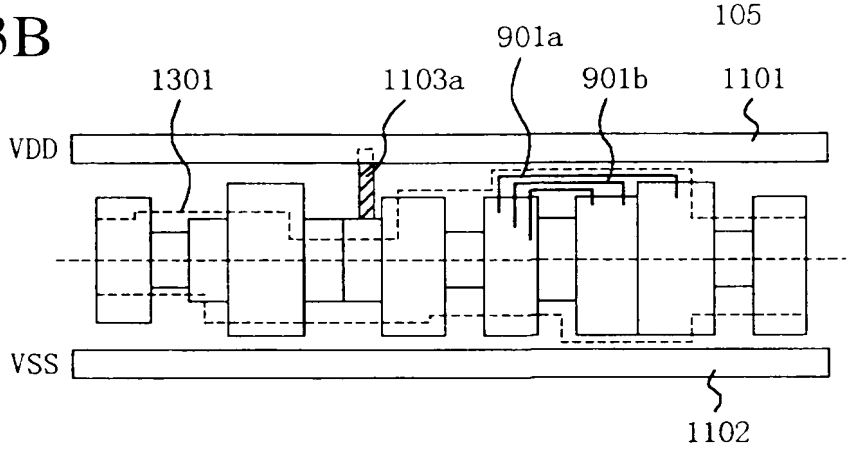

Fig. 13C

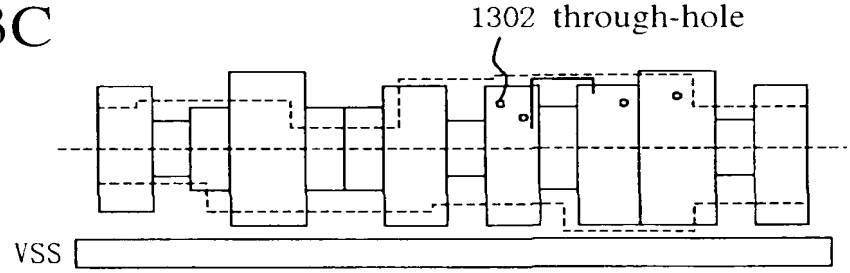

Fig. 13D

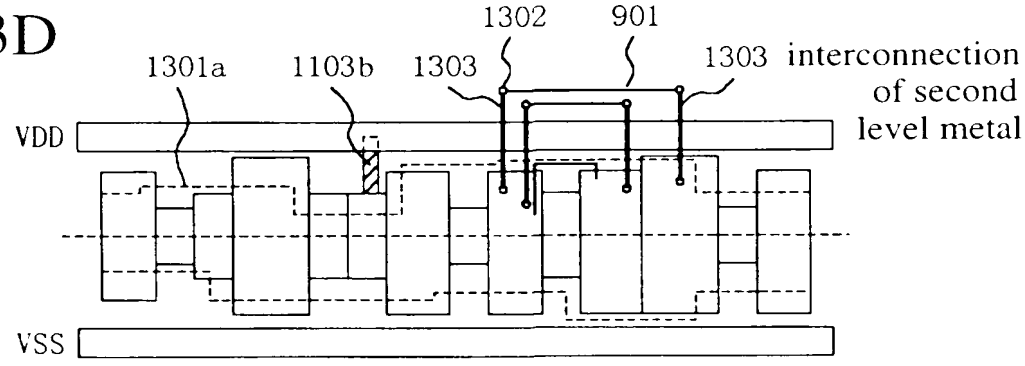

Fig. 14

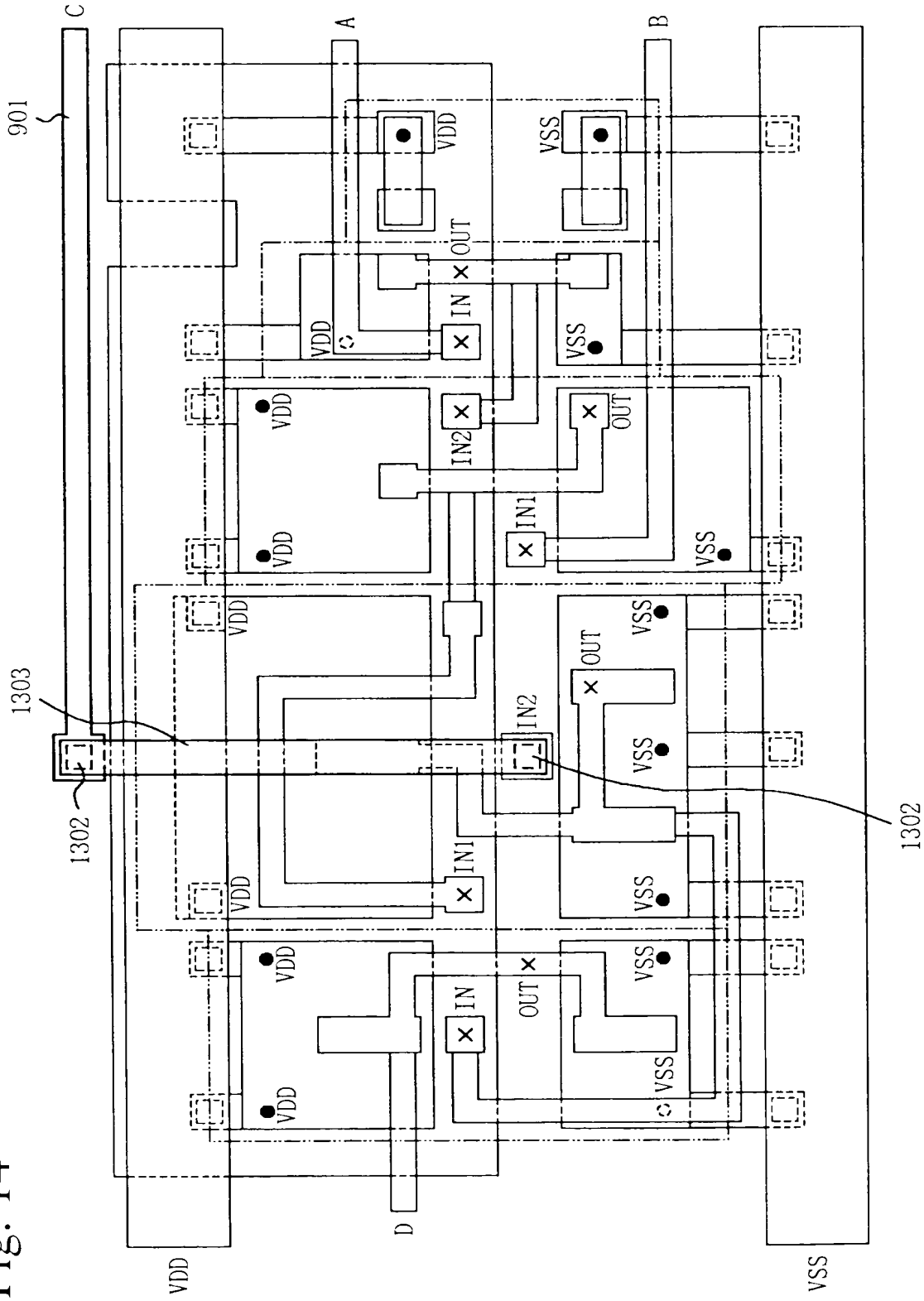

Fig. 15

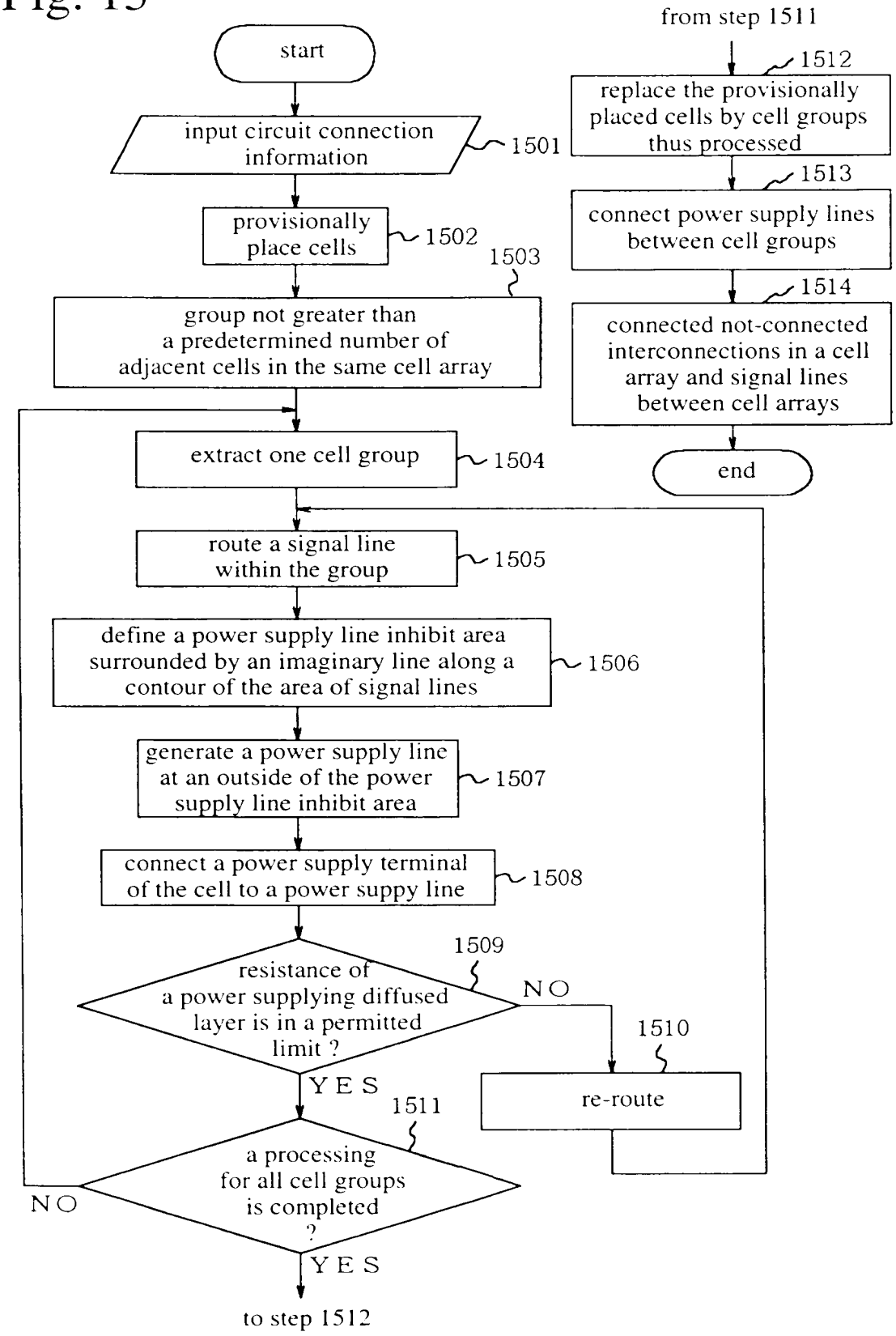
start
input circuit connection information
1501
provisionally place cells
1502
1503
group not greater than a predetermined number of adjacent cells in the same cell array
extract one cell group
1504
route a signal line within the group
1505
define a power supply line inhibit area surrounded by an imaginary line along a contour of the area of signal lines
1506
generate a power supply line at an outside of the power supply line inhibit area
1507
connect a power supply terminal of the cell to a power suppy line
1508
1509
resistance of a power supplying diffused layer is in a permitted limit ?
NO
1510
re-route
YES
1511
a processing for all cell groups is completed ?
NO
YES
to step 1512
from step 1511
1512
replace the provisionally placed cells by cell groups thus processed
1513
connect power supply lines between cell groups
1514
connected not-connected interconnections in a cell array and signal lines between cell arrays
end

Fig. 16A

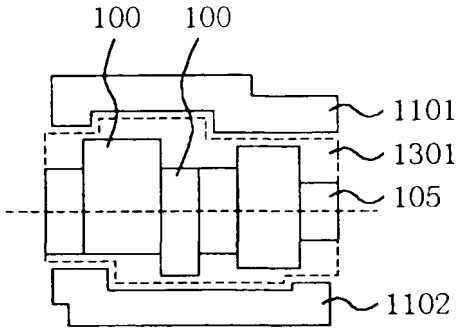

Fig. 16B

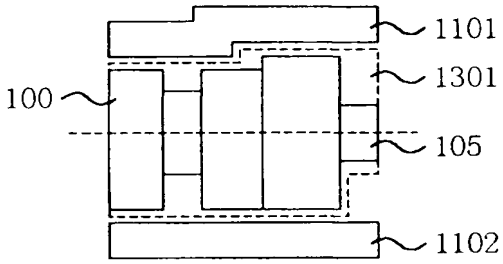

Fig. 16C

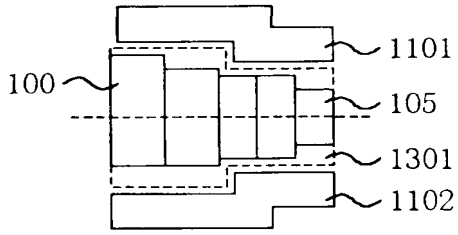

Fig. 16D

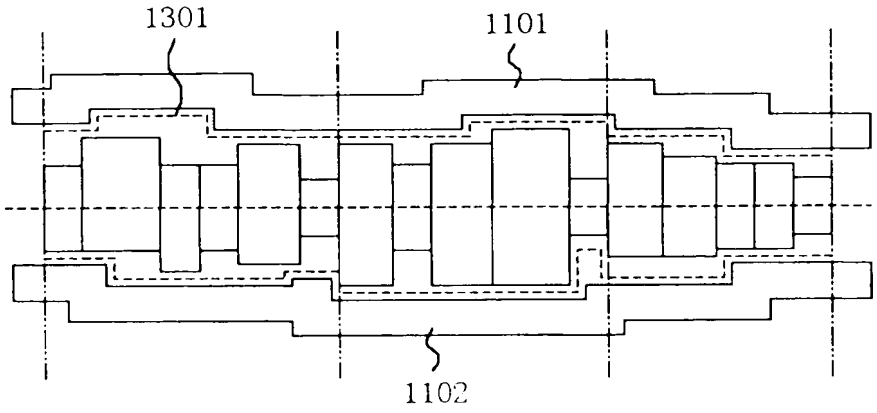

Fig. 17

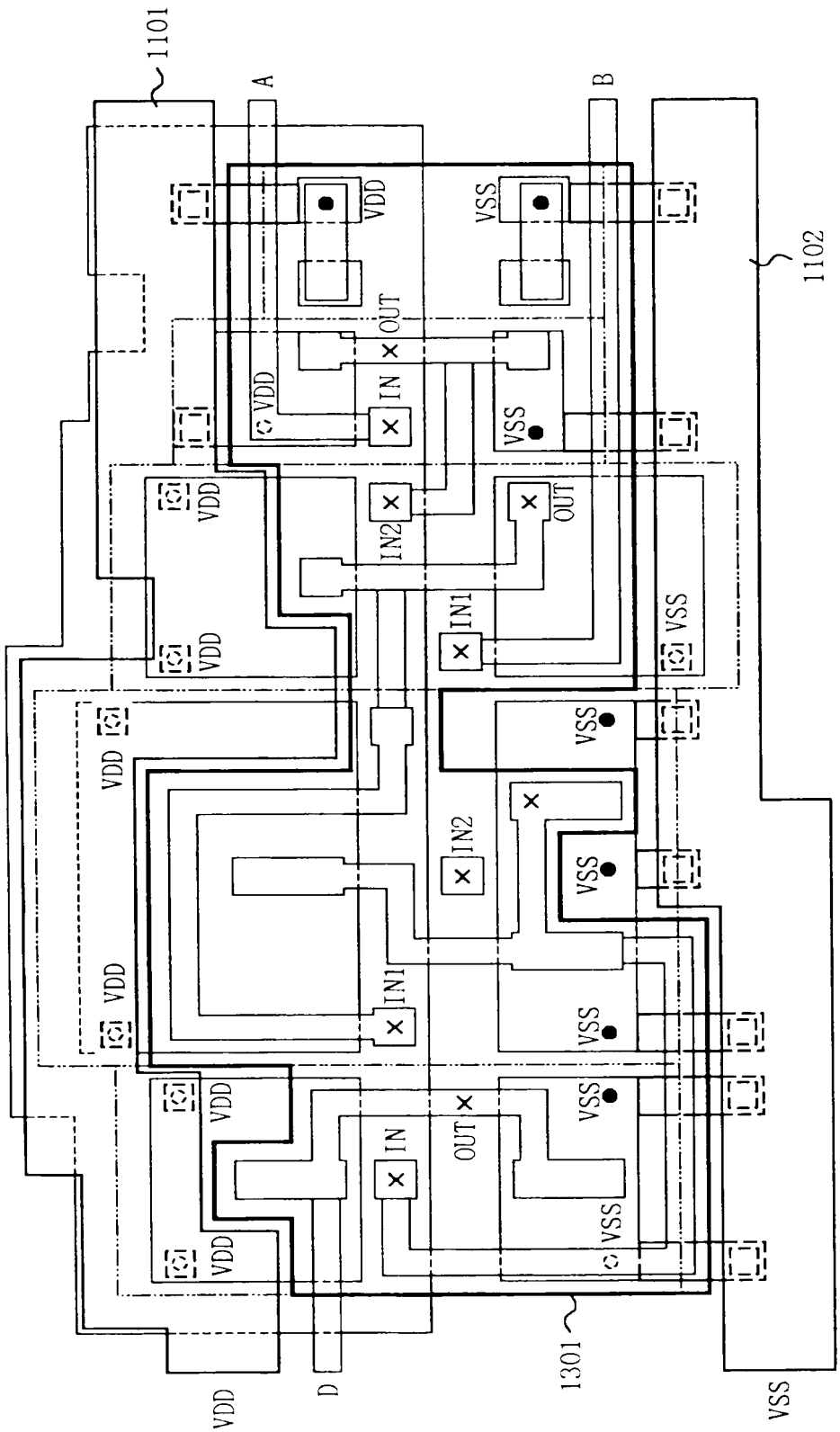

Fig. 18A
Prior Art

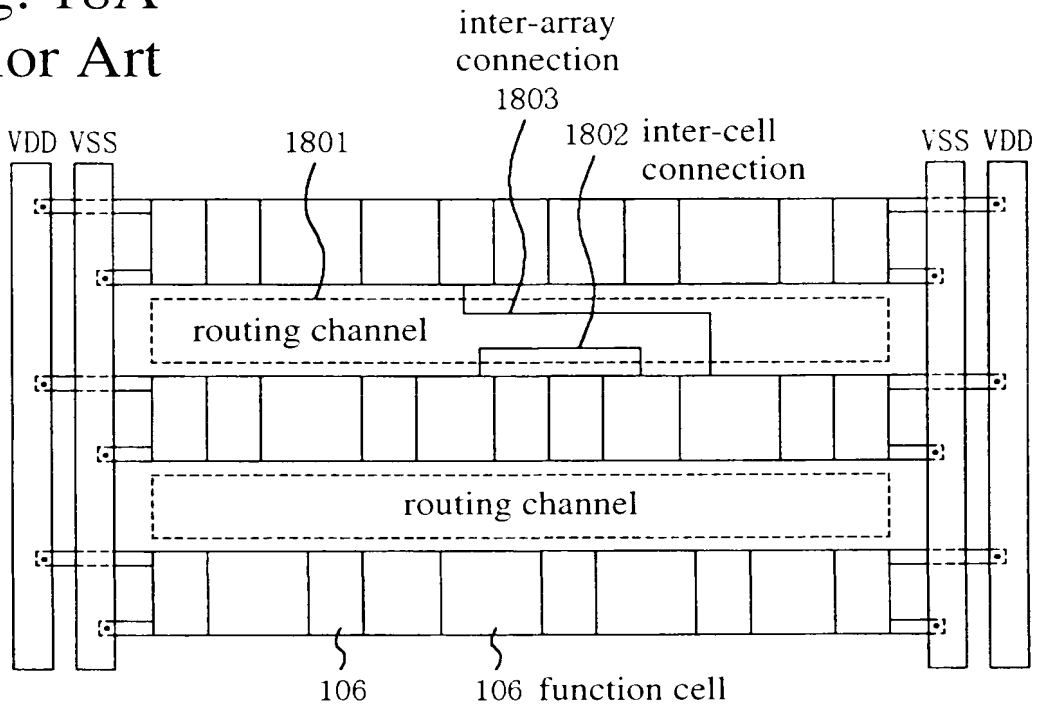

Fig. 18B
Prior Art

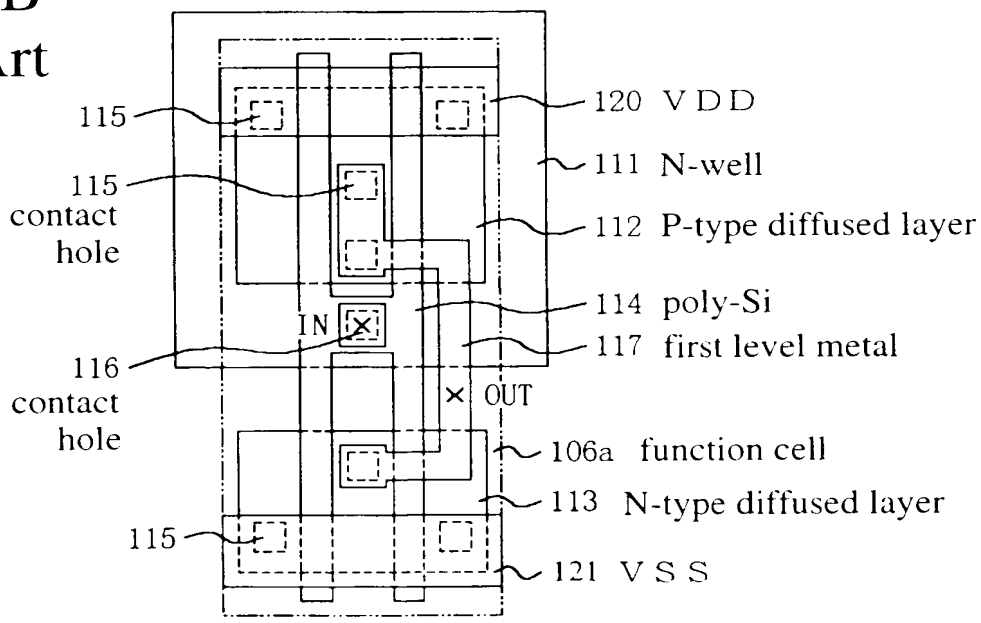

Fig. 19A
Prior Art

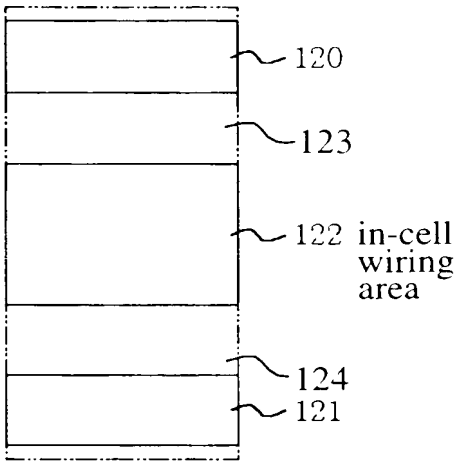

Fig. 19B
Prior Art

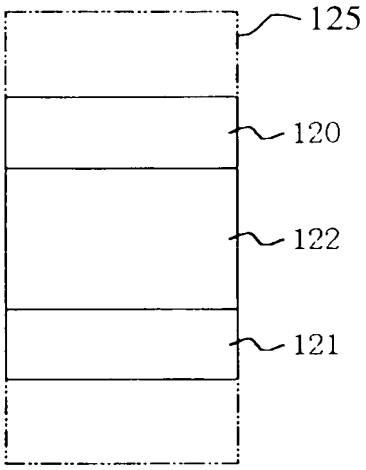

Fig. 19C
Prior Art